SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

Department of Artificial Intelligence and Data Science

(Common to IT, CSE, CYS)

QUESTION BANK

Academic Year 2025 – 2026(ODD SEMESTER)

III SEMESTER

AD3363-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

Regulation – 2023

Prepared by

Dr.A. Samydurai, Prof/CSE

Ms. Anslam Sibi, A.P(Sr.G)/CSE

Ms. M. Priyadharshini, A.P(O.G)/CSE

Mr. R. Danu, AP (O.G)/ AI&DS

Ms.R. Manjupriya, AP (O.G)/ AI&DS

Ms.M. Raghavi, AP (O.G)/CYS

Mr. Sivakumar K, AP (O.G)/IT

Ms.D. Nisha, AP (O.G)/IT

UNIT-I: COMBINATIONAL LOGIC

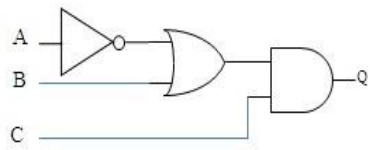
Combinational Circuits – Karnaugh Map - Analysis and Design Procedures – Binary Adder – Subtractor – Decimal Adder - Magnitude Comparator – Decoder – Encoder – Multiplexers - Demultiplexers.

PART-A

Q.no	Question	BTL	Competence
1	Find the Octal equivalent of the hexadecimal number DC.BA.	BTL2	Understanding
2	List two differences between combinational and sequential circuits.	BTL1	Remembering
3	Discuss the NOR operation with a truth table.	BTL1	Remembering
4	Write short notes on weighted binary codes.	BTL1	Remembering
5	Convert $(126)_{10}$ to Octal number and binary number.	BTL1	Remembering
6	Prove the following using Demorgan' theorem [(X+Y)'+(X+Y)']'= X+Y	BTL1	Remembering
7	Convert $(0.6875)_{10}$ to binary.	BTL1	Remembering
8	Implement AND gate using only NOR gate	BTL1	Remembering
9	State the principle of duality	BTL1	Remembering
10	How many cells are there in a 3-variable K-map?	BTL1	Remembering
11	Find the octal equivalent of hexadecimal numbers AB.CD.	BTL1	Remembering
12	Realize XOR gate using only 4 NAND gates.	BTL2	Understanding
13	Realize JK flip flop using D flip flop.	BTL1	Remembering
14	Convert the following hexadecimal numbers into decimal numbers: a)263, b)1C3	BTL1	Remembering
15	What is the significance of BCD code?	BTL1	Remembering
16	Simplify the expression: X = (A'+B)(A+B+D)D'.	BTL1	Remembering
17	Convert $(11001010)_2$ into gray code. b) Convert a Gray code 11101101 into binary code.	BTL1	Remembering
18	What are the outputs of a half adder?	BTL1	Remembering
19	Minimize the function using K-map: F=∑m(1,2,3,5,6,7).	BTL1	Remembering
20	Define Karnaugh map.	BTL1	Remembering
21	Plot the expression on K-map: F (w, x, y) =∑m (0, 1, 3, 5, 6) + d (2, 4).	BTL1	Remembering
22	Express x + yz as the sum of minterms	BTL1	Remembering
23	Simplify: a) Y = AB'D + AB'D' b) Z = (A'+B)(A+B).	BTL1	Remembering
24	Draw the truth table of a full adder.	BTL1	Remembering

PART-B

Q.no	Question	Mark	BTL	Competence
1(a)	Add, subtract and multiply the following numbers (110010)2 and(11101)2.	05	BTL1	Remembering
1(b)	State and prove De Morgan's theorems for 2-variables	05	BTL1	Remembering

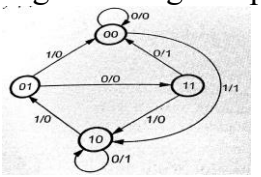
1(c)	Find complement of the following Boolean expression xyz'+ x'yz + z(xy+w)	06	BTL1	Remembering
2	Evaluate: (ABCD.1234)16 = (?)8 = (?)10 = (?)2 = (?)BCD = (?)5	03 03 05 05	BTL5	Evaluating
3(a)	Short notes on 1's and 2's complement	08	BTL1	Remembering
3 (b)	Explain the rules for Binary Addition and Subtraction using 1's & 2's complement. Give examples.	08	BTL5	Evaluating
4	Design an 8-to-3 priority encoder and explain how it works. Include the truth table and logic diagram.	16	BTL1	Remembering
5	Simplify the following switching function using karnaugh map method and realize expression using gates F(A,B,C,D) = ∑(0,3,5,7,8,9,10,12,15)	16	BTL2	Understanding
6	Examine how to minimize the function: F(A, B, C, D)=∑m(0,4,6,8,9,10,12) +∑d(2,13) and implement it using only NOR gates.	16	BTL 1	Remembering
7(a)	Simplify the Boolean function in Sum of Products(SOP) and Product of Sum(POS) F(w,x,y,z)=∑m(0,1,2,5,8,9,10).	08	BTL4	Analyzing
7(b)	Design the Boolean function in Karnaugh map and simplify it F(w,x,y,z)=∑m(0,1,2,4,5,6,8,9,12,13,14).	08	BTL6	Creating
8	Simplify the following Boolean expression in (a) Sum of Product (b) Product of Sum using Karnaugh map AC' + B'D + A'CD + ABCD.	08 08	BTL4	Analyzing
9(a)	Express the following function in sum of min-terms and product of max-terms: F(x,y,z)=x+yz.	08	BTL2	Understanding
9(b)	Convert the following logic system in to NAND gates only. 	08	BTL3	Applying

10(a)	Implement the following Boolean function with NAND-NAND logic F(A,B,C)= ∑m(0,1,3,5)	08	BTL6	Creating
10(b)	What is a demultiplexer? Explain how a 1-to-4 demultiplexer works using a circuit diagram.	08	BTL1	Remembering
11(a)	Plot the logical expression: ABCD + AB'C'D' + AB'C + AB on a 4 variable K-map; obtain the simplified expression from the map	08	BTL 3	Applying
11(b)	Express the function Y = A + B'C in canonical SOP and canonical POS form.	08	BTL 3	Applying
12(a)	Explain the procedure for obtaining NOR- NOR circuit for any AND-OR network with a suitable example.	08	BTL5	Evaluating

12(b)	Simplify the given Boolean function in POS form using k-map F(A,B,C,D) =ΠM(0,1,4,7,8,10,12,15)+d(2,6,11,14)	08	BTL4	Analyzing
13	Simplify the following switching function using Quine Mc Cluskey method and realize expression using gates F(A,B,C,D) = ∑(0,5,7,8,9,10,11,14,15)	16	BTL3	Applying
14	Simplify the function F(w,x,y,z)=∑m(2,3,12,13,14,15) using Tabulation method. Implement the simplified function using gates.	16	BTL4	Analyzing
15	Minimize the following function using Karnaugh map F (A, B, C, D) = ∑m(0,1,2,3,4,5,6,11,12,13) and implement with logic gates.	16	BTL4	Analyzing
16	Minimize the expression using K-map and Quine Mccluskey method Y= A'BC'D + A'BC'D+ABC'D'+ABC'D'+AB'C'D+A'B'CD'	16	BTL2	Understanding
17(a)	Explain the procedure for obtaining NAND- NAND circuit for any AND-OR network with a suitable example.	08	BTL5	Evaluating
17(b)	Implement Y= (A'B+AB') (C+D') using NOR gates.	08	BTL3	Applying
18(a)	Deduce FACE16 in its binary, octal and decimal equivalent.	04	BTL5	Evaluating
18(b)	Simplify the function F=xy+x'y'z'+x'yz'.	02		
18(c)	Interpret the logical expression using K-map in SOP and POS form: F (A, B, C, D) =∑m (0, 2, 3, 6, 7) + d (8, 10, 11, 15).	10		
19	Simplify the Boolean function using QuineMcCluskey method: F (A, B, C, D,E) = ∑m (0,1,3,7,13,14,21,26,28)+ ∑d(2,5,9,11,17,24)	16	BTL5	Evaluating
20	Reduce the following function using K-map technique. i) f (A, B, C) = ∑m (0,1,3,7) + ∑d (2,5) ii) F (w,x,y,z) = ∑m (0,7,8,9,10,12) + ∑d (2,5,13)	16	BTL5	Evaluating
21	Simplify the following Boolean function F using Tabulation method. i) F (A, B, C, D) = ∑m (0,6,8,13,14), d (A, B, C, D) = ∑m (2,4,10) ii) F (A, B, C, D) = ∑m (1,3,5,7,9,15), d (A, B, C, D) = ∑m (4,6,12,13)	16	BTL5	Evaluating
22	Implement the following function using 8 to 1 multiplexer f(a,b,c,d)= ∑m(0,1,3,5,9,12,14,15)	16	BTL5	Evaluating
23	Construct 16X1 multiplexer with two 8X1 and 2X1 multiplexer. Use Block diagrams.	16	BTL3	Applying

UNIT II - SYNCHRONOUS SEQUENTIAL LOGIC
Introduction to Sequential Circuits – Flip-Flops – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design – Moore/Mealy models, state minimization, state assignment, circuit implementation - Registers – Counters.
PART-A

Q.no	Question	BTL	Competence
1	Define the excitation table of a flip-flop.	BTL1	Remembering
2	What are the classifications of sequential circuits?	BTL1	Remembering
3	Define Latch.	BTL1	Remembering
4	Define a flip flop.	BTL1	Remembering
5	What are the different types of flip-flop?	BTL1	Remembering
6	Define registers.	BTL1	Remembering
7	What is the characteristic equation of a D flip-flop?	BTL1	Remembering
8	What is the difference between positive edge and negative edge triggering?	BTL1	Remembering
9	What is the operation of JK flip-flop?	BTL1	Remembering
10	What is the operation of T flip-flop?	BTL1	Remembering
11	Define race around condition	BTL1	Remembering
12	What is triggering? What is the need for trigger in flip-flop?	BTL2	Understanding
13	What is meant by level and edge-triggering?	BTL1	Remembering
14	Draw the logic diagram and write the function table of D Latch.	BTL1	Remembering
15	How do you eliminate race around condition in JK flip flop?	BTL1	Remembering
16	Define rise time	BTL1	Remembering
17	Define fall time.	BTL1	Remembering
18	Define skew and clock skew.	BTL1	Remembering
19	State the difference between latches and flip flops.	BTL2	Understanding
20	What is mealy and Moore circuit? Or what are the models used to represent clocked sequential circuits?	BTL1	Remembering
21	What is counter and List its types?	BTL2	Understanding
22	Mention one method of assigning states.	BTL1	Remembering
23	State the Steps or Design procedure for Synchronous Counter.	BTL2	Understanding
24	What is modulo-N counter?	BTL1	Remembering

PART-B				
Q.no	**Question**	**Mark**	**BTL**	**Competence**
1	Explain the operation of flipflops.	16	BTL 5	Evaluating
2	Write short notes on Mealy and Moore models in sequential circuits	16	BTL2	Understanding
3	Explain the operation of a 4-bit binary ripple counter.	16	BTL2	Understanding
4	Explain about Modulo 16 /4 bit Ripple Down counter.	16	BTL 5	Evaluating
5	Explain about Asynchronous Up/Down counter.	16	BTL 5	Evaluating
6	Explain about 4-bit Synchronous up-counter.	16	BTL 5	Evaluating
7	Explain about 4-Bit Synchronous down counter.	16	BTL 5	Evaluating
8	Explain about Modulo 8 Synchronous Up/Down Counter.	16	BTL 5	Evaluating
9	Design a 3-bit binary counter using T-flip flops.	16	BTL 5	Evaluating
10	Design of a Synchronous Modulus-Six Counter Using SR Flip-Flop	16	BTL 5	Evaluating
11	What are registers? Construct a 4 bit register using D-flip flops and explain the operations on the register.	16	BTL 5	Evaluating
12	Explain how to analyze and design a clocked sequential circuit using flip-flops. Give an example and show the steps involved.	16	BTL2	Understanding
13	Explain about Johnson and Ring counter	16	BTL2	Understanding
14	Design the sequential circuit specified by the following state diagram using T flip flops 	16	BTL 5	Evaluating
15	Explain the working of SR, JK, D, and T flip-flops. Draw the operation and excitation tables for each flip-flop with logic diagrams.	16	BTL2	Understanding
16(a)	Explain about synchronous and asynchronous sequential Circuit.	08	BTL3	Applying
16(b)	Explain the working procedure of 3 bit parallel- in serial-out shift register construct the state table.	08	BTL1	Remembering
17	Explain the different types of shift registers with neat diagram.	16	BTL2	Understanding
18	Design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000 using D flip-flop.	16	BTL6	Creating

19	Design sequence detector that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line and produces an output whenever this sequence is detected.	16	BTL6	Creating
20	A sequential circuit with two D flip-flops A and B, one input x , and one output z is specified by the following next state and output equations: A(t+1) = A'+B; B(t+1)=B'X; Z =A+B' Draw the logic diagram of the circuit. (05) Derive the state table. (05) Draw the state diagram of the circuit. (06)	16	BTL5	Evaluating
21	Analyze and design a sequential circuit with two T Flip flop A and B, one input x and one output z is specified by the following next stateand output equation is A(t+1)= BX'+B'X B(t+1)=AB+BX+AX Z=AX'+A'B'X Draw thelogic diagram of the circuit (05) List the state table for the sequential circuit (05) Draw the Corresponding state diagram (06)	16	BTL6	Creating
22	A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations: A (t+1) = AX+BX; B (t+1) = A'X; Y= (A+B) X'. (i) Draw the logic diagram. (05) (ii) Construct the state table. (05) **(iii)** Draw the state diagram. (06)	16	BTL 6	Creating

UNIT - III COMPUTER FUNDAMENTALS

Functional Units of a Digital Computer: Von Neumann Architecture – Operation and Operands of Computer Hardware Instruction – Instruction Set Architecture (ISA): Memory Location, Address and Operation – Instruction and Instruction Sequencing – Addressing Modes, Encoding of Machine Instruction – Interaction between Assembly and High Level Language.

PART – A

Q. No.	Questions	BT Level	Competence
1	What are the five components of computer system?	BTL1	Remembering
2	What is memory hierarchy?	BTL1	Remembering
3	What is the function of ALU?	BTL1	Remembering
4	What is the function of control unit?	BTL1	Remembering
5	What are basic operations of a computer memory?	BTL1	Remembering
6	List out the operations of the computer.	BTL1	Remembering
7	What is instruction set architecture	BTL2	Understanding
8	State Amdahl's law.	BTL2	Understanding
9	Define Stored Programmed Concept.	BTL2	Understanding
10	What are the registers generally contained in the processor?	BTL2	Understanding
11	**Describe** about the various logical operators.	BTL1	Understanding
12	What is the purpose of program counter?	BTL1	Understanding
13	Differentiate write back and write through?	BTL2	Understanding
14	Why cache memory is required?	BTL2	Understanding
15	Define Register addressing mode with an example.	BTL2	Understanding
16	What is relative addressing mode with an example?	BTL2	Understanding
17	What is indirect addressing mode?	BTL2	Understanding
18	What is indexed addressing mode?	BTL2	Understanding
19	List out the methods used to improve system performance	BTL2	Understanding
20	List the phases, which are included in the each instruction cycle?	BTL2	Understanding

21	What are the two major steps in processing an instruction? (Or) Write the two steps that are common to implement any type of instruction.	BTL2	Understanding
22	What are the speedup techniques available to increase the performance of a computer?	BTL2	Understanding
23	Distinguish between auto increment and auto decrement addressing mode	BTL2	Understanding
24	What are the limitations of assembly language?	BTL2	Understanding

PART – B

Q.no	Questions	Mark	BTL	Competence
1	Explain in detail about the components of a computer system.	16	BTL5	Evaluating
2	Explain about operations operands of computer hardware instruction.	16	BTL5	Evaluating
3	Discuss about ISA.	16	BTL6	Creating
4	Explain in details about RISC and CISC instruction set architecture and its difference	16	BTL6	Creating
5	What is the need for addressing in a computer system? Analyze the different addressing modes with suitable examples.(Or) Explain direct, immediate, relative and indexed addressing modes with examples.(Or) Identify the addressing mode involved in the instruction XOR r1 r2+ 100 r1 and determine the resultant stored in register R1 if all of its bit were 1'st initially .	16	BTL2	Analyzing
6.	Consider the computer with three instruction classes and CPI measurements as given below and instruction counts for each instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 4 GHZ. Which code sequence will execute faster according to execution time?	16	BTL6	Creating
7	Explain about encoding of machine instruction.	16	BTL5	Evaluating
8	Explain the concept of interaction between assembly and high level language	16	BTL3	Applying
9	With a neat diagram, describe about Von Newmann Architecture	16	BTL3	Applying
10	What is an addressing mode? Outline the types of Addressing mode with an example.	16	BTL3	Applying
11	Analyze about the functional unit of Digital Computer? Discuss about instruction cycle.	16	BTL4	Analyze
12	Describe instruction sequencing and branching with example	16	BTL4	Analyze

13	Explain any four addressing modes with example.(13)	16	BTL5	Evaluating
14	Give the comparison between compiler and interpreter.	16	BTL4	Analyze
15	Give the comparison between machine level, and assembly level and high level languages.	16	BTL4	Analyze
16	How to encode assembly instructions into 32-bit words? Analyze with examples.	16	BTL4	Analyze
17	Explain the following: i) Byte addressability, ii) Big-endian assignment, iii) Little-endian assignment.	5 5 6	BTL5	Evaluating
18	Difference between assembler and compiler design and illustrate its working principles	16	BTL5	Evaluating
19	Elaborate the different types of addressing modes with a suitable example.	16	BTL5	Evaluating
20	Explain the centralized and distributed bus system in computer organization.	16	BTL 2	Understand

UNIT - IV: PROCESSOR

I/O Instruction Execution – Building a Data Path – Designing a Control Unit – Hardwired Control, Microprogrammed Control – Pipelining – Data Hazard – Control Hazards.

PART – A

Q.No	Questions	BTL	Competence
1	What is the primary function of a processor in a computer system?	BTL 2	Understanding
2	Define instruction execution in the context of a processor.	BTL 1	Remembering
3	What is the significance of instruction fetch in instruction execution?	BTL 2	Understanding
4	What is a data path in a processor?	BTL 2	Understanding
5	What is the purpose of an ALU in a data path?	BTL 2	Understanding
6	Explain the role of a control unit in a processor.	BTL 2	Understanding
7	Explain the term 'instruction decode' in the execution cycle.	BTL 2	Understanding
8	What is a branch prediction?	BTL 2	Understanding
9	What is hardwired control?	BTL 2	Understanding
10	Define microprogrammed control.	BTL 1	Remembering
11	Differentiate between hardwired control and microprogrammed control.	BTL 1	Analyzing
12	What is pipelining in a processor?	BTL 1	Understanding
13	Define the term 'pipeline stage.'	BTL 1	Understanding

14	What is a pipeline stall?	BTL 2	Understanding
15	What is meant by instruction throughput in pipelining?	BTL 1	Understanding
16	Define the term 'control signal' in a processor.	BTL 1	Remembering
17	What is a register file in a processor?	BTL 2	Understanding
18	Explain the term 'pipeline hazard.'	BTL 2	Understanding
19	Explain the concept of a data hazard.	BTL 2	Understanding
20	What is a control hazard?	BTL 1	Remembering
21	Define pipelining in computer architecture.	BTL 1	Remembering
22	List the types of data hazards in pipelining.	BTL 1	Remembering
23	State the function of a control unit in a CPU.	BTL 1	Remembering
24	Define microprogrammed control.	BTL 1	Remembering

PART – B

Q. No	Questions	Marks	BT Level	Competence
1	Apply the concepts of data path design to a specific CPU architecture of your choice. Explain how the various components such as the ALU, registers, and control unit are interconnected and managed within this architecture.	16	BTL3	Applying
2	Discuss how pipeline stages can lead to data hazards and the techniques used to mitigate these hazards.	16	BTL3	Applying
3	Generalize the principles of hardwired and microprogrammed control units.	16	BTL3	Applying
4	Estimate the performance impact of control hazards in a pipelined architecture. Discuss the various techniques used to minimize these hazards and how they affect overall CPU performance.	16	BTL3	Applying
5	Demonstrate the process of designing a microprogrammed control unit for a simple instruction set.	16	BTL3	Applying
6	Analyse the impact of pipelining on processor performance.	16	BTL 4	Analyzing
7	Compare hardwired control and microprogrammed control in terms of design complexity, flexibility, and performance.	16	BTL 4	Analyzing
8	Examine the causes and solutions for data hazards in pipelined processors.	16	BTL 4	Analyzing
9	Distinguish between control hazards and data hazards, providing examples of each.	16	BTL 4	Analyzing
10	Classify the different types of data paths used in computer architecture and discuss their respective advantages and disadvantages.	16	BTL 4	Analyzing
11	Construct a detailed data path for a simple RISC processor. Include all necessary components such as registers, ALU, memory units, and control signals.	16	BTL5	Evaluating

12	Develop a comprehensive microprogrammed control unit for a basic CPU. Explain the control signals and microinstructions required for executing various instructions.	16	BTL5	Evaluating
13	Design a hardwired control unit for a simple instruction set. Describe the state diagram and the logic equations needed to generate the control signals.	16	BTL5	Evaluating
14	Modify a basic pipelined processor to handle data hazards. Discuss the techniques such as forwarding, stalling, and hazard detection units used to resolve these hazards.	16	BTL5	Evaluating
15	Compare and contrast different techniques such as branch prediction, delayed branching, and branch target buffers.	16	BTL5	Evaluating
16	Choose a Data Path Design for a Given Processor Architecture and Justify Your Choice.	16	BTL6	Creating
17	Decide on the Control Unit Design for a Processor and Explain Your Decision.	16	BTL6	Creating
18	Justify the Use of Pipelining in Modern Processors and Explain How It Improves Performance.	16	BTL6	Creating
19	Choose an Approach to Handle Data Hazards in a Pipeline and Explain Its Mechanism and Effectiveness.	16	BTL6	Creating
20	Explain Different Techniques to Handle Control Hazards in Pipelined Processors and Choose the Most Effective One.	16	BTL6	Creating

UNIT – V : MEMORY AND I/O

Memory Concepts and Hierarchy – Memory Management – Cache Memories: Mapping and Replacement Techniques – Virtual Memory – DMA – I/O – Accessing I/O: Parallel and Serial Interface – Interrupt I/O – Interconnection Standards: USB, SATA

PART – A

Q.N	Questions	BTL	Competence
1	What is memory hierarchy?	BTL 2	Understanding
2	Define memory management.	BTL 1	Remembering
3	What is cache memory?	BTL 2	Understanding
4	Explain direct mapping in cache memory.	BTL 2	Understanding
5	What is a cache replacement policy?	BTL 2	Understanding
6	Define virtual memory.	BTL 1	Remembering
7	What does DMA stand for?	BTL 2	Understanding
8	What is the purpose of I/O in a computer system?	BTL 2	Understanding
9	Differentiate between parallel and serial interfaces.	BTL 1	Remembering
10	What is an interrupt in the context of I/O?	BTL 2	Understanding
11	What does USB stand for?	BTL 2	Understanding
12	What is the full form of SATA?	BTL 2	Understanding

13	What is meant by memory access time?	BTL 2	Understanding
14	Define page in memory management.	BTL 1	Remembering
15	What is cache hit and miss?	BTL 2	Understanding
16	Explain the concept of a page table.	BTL 2	Understanding
17	Explain the structure and functioning of an arithmetic logic unit (ALU) within a data path.	BTL 2	Understanding
18	Discuss the design and working of a control unit in a processor.	BTL 1	Remembering
19	Discuss the challenges and solutions in designing a control unit for a complex instruction set.	BTL 2	Understanding
20	Explain the concept of plug and play in USB.	BTL 2	Understanding
21	Differentiate write back and write through.	BTL 1	Remembering
22	What is hit time?	BTL 1	Remembering
23	Which signal is used to notify the processor that the transfer is completed? Define.	BTL 1	Remembering
24	Specify the three types of the DMA transfer techniques?	BTL 1	Remembering

PART – B

Q.No	Questions	Marks	BTL	Competence
1	How does direct mapping in cache memory improve data retrieval speed? Provide a real-world example.	16	BTL3	Applying
2	Explain how virtual memory management supports multitasking in operating systems. Give one practical example.	16	BTL3	Applying
3	Compare DMA and interrupt-driven I/O in terms of their impact on CPU utilization and system performance.	16	BTL3	Applying
4	Estimate the storage capacity difference between USB 2.0 and USB 3.0 for transferring a 2 GB file.	16	BTL3	Applying
5	Describe the role of SATA in connecting storage devices to a computer.	16	BTL3	Applying
6	Analyse the role of cache memories in computer systems, comparing and contrasting different mapping and replacement techniques.	16	BTL 4	Analyzing
7	Compare virtual memory management with direct memory access (DMA), examining their respective roles and functionalities in computer systems.	16	BTL 4	Analyzing
8	Examine the characteristics and functionalities of USB and SATA interconnection standards, highlighting their respective strengths and applications in modern computing.	16	BTL 4	Analyzing
9	Distinguish between parallel and serial interfaces in I/O operations, highlighting their architectures, advantages, and limitations.	16	BTL 4	Analyzing
10	Analyze how virtual memory works with paging and segmentation. Compare the advantages and disadvantages of both techniques.	16	BTL 4	Analyzing
11	Compare and contrast different cache mapping techniques (Direct, Associative, Set-Associative). Include diagrams and examples.	16	BTL 4	Analyzing
12	Develop a comparison between direct memory access (DMA) and interrupt-driven I/O.	16	BTL5	Evaluating

13	Design a virtual memory system outline, including key components like paging and swapping.	16	BTL5	Evaluating
14	Modify a cache memory configuration for better performance, specifying changes in size or associativity.	16	BTL5	Evaluating
15	Formulate a summary of USB and SATA standards, highlighting their key features and typical uses in computing.	16	BTL5	Evaluating
16	Choose an example of a cache mapping technique and explain its advantages.	16	BTL6	Creating
17	Decide between virtual memory and cache memory for optimizing system performance. Justify your choice.	16	BTL6	Creating
18	Justify the importance of DMA in reducing CPU workload during data transfers. Provide an example.	16	BTL 6	Creating
19	Choose a cache replacement policy and explain how it manages memory efficiency.	16	BTL6	Creating
20	Explain the advantages of USB and SATA in peripheral connectivity. Compare their speeds briefly.	16	BTL6	Creating